## AMENDMENTS TO THE CLAIMS:

Complete Claim Listing:

Claims 1 - 30 (Canceled)

31. (Currently Amended) A memory device comprising:

a substrate;

a gate located over the substrate;

a first charge storage structure located over an insulating layer on the substrate, at least a portion of the first charge structure located under a first portion of the gate,

a second charge storage structure located over the substrate, at least a portion of the second charge storage structure located under a second portion of the gate, the second charge storage structure is located apart from the first charge storage structure; ;

wherein the gate includes a third portion located between the first portion of the gate and the second portion of the gate;

a gate dielectric, a first portion of the gate dielectric located between the substrate and the first charge storage structure, a second portion of the gate dielectric located between the substrate and the second charge storage structure, a third portion of the gate dielectric located between the substrate and the third portion of the gate, wherein the third portion of the gate dielectric at a location where the gate is closest to the substrate, has a thickness that is different from a thickness of first portion of the gate dielectric and a thickness of the second portion of the gate dielectric.

32. (Original) The memory device of claim 31 wherein the thickness of the third portion of the gate dielectric at the location is less than the thickness of the first portion of the gate dielectric and less than the thickness of the second portion of the gate dielectric.

33. (Original) The memory device of claim 31 wherein the thickness of the third portion of the gate dielectric at the location is greater than the thickness of the first portion of the gate dielectric and is greater than the thickness of the second portion of the gate dielectric.

34. (Original) The memory device of claim 31 wherein the first charge storage structure and the second charge storage structure each include a plurality of discrete charge storage elements.

35. (Original) The memory device of claim 31 wherein a width of the first charge storing structure and a width of the second charge storing structure is less than a minimum feature size.

36. (Original) The device of claim 31 wherein each of the first and second charge storage structures is for storing one bit of information.

Claims 37 - 39 (Canceled)